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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

B2

Office Action Summary	Application No.	Applicant(s)	
	10/763,664	HIRST, MARK	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-16,18-22 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-16,18-22 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-9, 10-16, 18-22 and 25-27 have been considered but are moot in view of the new ground(s) of rejection.

Response to Amendment

2. The amendment filed 10/31/2005 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the first intrinsic diode having an anode coupled to the first drain and a cathode coupled to the first source, a second intrinsic diode having an anode coupled to the second drain and a cathode coupled to the second source, a third diode having an anode coupled to the first source and a cathode coupled to the first drain and a fourth diode having an anode coupled to the second drain and a cathode coupled to the second drain of claim 5.

Applicant is required to cancel the new matter in the reply to this Office Action.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first intrinsic diode having an anode coupled to the first drain, a second intrinsic diode having an anode coupled to the second drain, a third diode having an anode coupled to the first source and a fourth diode having an anode coupled to the second drain of claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 5-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added matter is as follows: the first intrinsic diode having an anode coupled to the first drain and a cathode coupled to the first source, a second intrinsic diode having an anode coupled to the second drain and a cathode coupled to the second source, a third diode having an anode coupled to the first source and a cathode coupled to the first drain and a fourth diode having an anode coupled to the second drain and a cathode coupled to the second drain of claim 5.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-4, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,236,192) in view of Sharples et al (US 6,521,973).

Claims 1-4; Suzuki et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate; a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain. The FETS are N type MOSFETS and power MOSFETs. The first and second diodes include turn-on voltages less than or equal to 1.2 volts.

However, Suzuki et al do not disclose more diodes connected in parallel to the intrinsic diodes.

Sharples teaches that the parasitic diode is problematic in the case of an insulated-gate field-effect transistor (termed MOSFET). Because this diode is a bipolar component, it is subject to charge storage effects. It generally has a slow reverse recovery time, which can cause switching losses in operation of the MOSFET. To solve this problem of a slow reverse recovery time, Sharples teaches using a transistor circuit arrangement with an additional external diode of fast recovery time coupled in parallel relationship to the parasitic diode. This fast-recovery diode provides the inverter with a reverse current path external to the MOSFET and in place of the suppressed slow-recovery internal (parasitic) diode of the MOSFET.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to connect an external diode to the source and drains of the MOSFETs in the circuit of Suzuki et al as taught by Sharples in order to provide a reverse current path external

to the MOSFET and in place of the suppressed slow-recovery internal (parasitic) diode of the MOSFET.

Claims 25 and 26; Suzuki et al disclose a method of switching alternating current comprising: receiving alternating current (AC) from a source; switching the alternating current utilizing a MOSFET switch having two MOSFET devices with coupled sources and coupled gates and diodes anti-parallel to each MOSFET device; and controlling the switching of the alternating current, by the MOSFET switch, at frequencies greater than 200 Hz. Further comprising providing switched AC to a load.

However, Suzuki et al do not disclose two diodes connected in parallel to the MOSFET diodes.

Sharples teaches that the parasitic diode is problematic in the case of an insulated-gate field-effect transistor (termed MOSFET). Because this diode is a bipolar component, it is subject to charge storage effects. It generally has a slow reverse recovery time, which can cause switching losses in operation of the MOSFET. To solve this problem of a slow reverse recovery time, Sharples teaches using a transistor circuit arrangement with an additional external diode of fast recovery time coupled in parallel relationship to the parasitic diode. This fast-recovery diode provides the inverter with a reverse current path external to the MOSFET and in place of the suppressed slow-recovery internal (parasitic) diode of the MOSFET.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to connect an external diode to the source and drains of the MOSFETs in the circuit of Suzuki et al as taught by Sharples in order to provide a reverse current path external

to the MOSFET and in place of the suppressed slow-recovery internal (parasitic) diode of the MOSFET.

8. Claims 8, 9, 11, 13-16, 18-21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,236,192) in view of Bijlenga (US 5,946,178).

Claims 8, 9, 11, 13 and 14; Suzuki et al disclose an alternating current switching circuit including; a fist Field Effect Transistor (FET) having a first source, a first gate and a first drain, a second FET having, a second drain, a second source coupled to the first source and a second gate coupled to the first gate, a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain; and a switch control circuit coupled to the first gate and the second gate and coupled to the first source and the second source, the switch control circuit to facilitate operation of the alternating current switching circuit at frequencies greater than 200 Hz. A load is coupled to the alternating current switching circuit; the switch control circuit uses pulse width modulation. Filtering circuitry at the load. The switch control circuit is configured to operate the alternating current switching circuit at frequencies greater than 20 kHz.

However, Suzuki et al do not disclose a snubber circuit with one resistor in series with one capacitor; wherein the snubber circuit connects the first drain and the second drain. Bijlenga teaches connecting a snubber circuit across a two transistor-diode circuit; and wherein the snubber circuit comprises one resistor (R2) in series with one capacitor (C2) in order to dissipate excess energy and is also effective with respect to overvoltages.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize one resistor and one capacitor in series and coupled to the first drain and the second drain of the alternating current switching circuit to dissipate energy in the alternating current switching circuit as taught by Bijlenga.

Claims 15, 16 and 18-21; Suzuki et al disclose an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first gate, a first drain, and a common source; a second FET having a second gate, a second drain and the common source; a first diode having a first anode coupled to the common source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the common source and a second cathode coupled to the second drain. The first gate is coupled to the second gate and wherein the alternating current switching circuit further comprises a switch control circuit coupled to the coupled gates and the common source, the switch control circuit to facilitate operation of the alternating current switching circuit at frequencies greater than 200 Hz. The first FET and the second FET are power MOSFETS. The first FET and the second FET are N-type MOSFETs.

However, Suzuki et al do not disclose a snubber circuit with one resistor in series with one capacitor; wherein the snubber circuit connects the first drain and the second drain.

Bijlenga teaches connecting a snubber circuit across a two transistor-diode circuit; and wherein the snubber circuit comprises one resistor (R2) in series with one capacitor (C2) in order to dissipate excess energy and is also effective with respect to overvoltages.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize one resistor and

one capacitor in series and coupled to the first drain and the second drain of the alternating current switching circuit to dissipate energy in the alternating current switching circuit as taught by Bijlenga.

Claim 27; Suzuki et al disclose a method of switching alternating current comprising: receiving alternating current (AC) from a source; and applying the alternating current across drains of two MOSFET devices of a switch, where the two MOSFET device having a common source region, and their gates are coupled together, and the switch further having diodes that are anti-parallel to each MOSFET device, flowing the alternating current though the common source region.

However, Suzuki et al do not disclose a snubber circuit connected across the drains. Bijlenga teaches connecting a snubber circuit across a two transistor-diode circuit in order to dissipate excess energy and is also effective with respect to overvoltages.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize a snubber circuit connected across the drains of the two MOSFETs in order to dissipate energy in the switches as taught by Bijlenga.

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,236,192) in view of Brulhart et al (US 6,259,306).

Suzuki et al disclose the claimed subject matter in regards to claim 8 supra, except for charge pump circuitry coupled to an alternating current power source and the switch control circuit.

Brulhart et al teach using charge pump circuitry (510, 520) coupled to switch control circuitry (500a , 500b) to drive an alternating current switching circuit in order to provide the proper voltage to the gates of the alternating current switching circuit transistors.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize charge pump circuitry coupled to an alternating current power source and the switch control circuit in order to provide the proper voltage to the gates of the alternating current switching circuit transistors as taught by Brulhart et al.

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,236,192) in view of Sugawara (US 5,635,826).

Claim 22; Suzuki et al disclose the claimed subject matter in regards to claim 15 supra, except for a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

Sugawara teach using a device (6) having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

However, the device of Sugawara uses more than four pins since Sugawara is driving two alternating current switching circuits. It is clearly obvious that if Sugawara were to drive only one alternating current switching circuit then only four pins would be required. A first pin would be coupled to the first and the second gate as shown in figure 1, a second pin coupled to the

common source as shown in figure 1, a third pin coupled to the first drain (at L1 and coupled through switch 7) and a fourth pin coupled to the second drain as shown in figure 1.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain in order to drive the alternating current switching circuit as taught by Sugawara.

11. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloomer (US 4,567,425) in view of Sharples et al (US 6,521,973).

Claims 1-4; Bloomer discloses an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first source, a first gate and a first drain; a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate; a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain. The FETS are N type MOSFETS and power MOSFETs. The first and second diodes include turn-on voltages less than or equal to 1.2 volts.

However, Bloomer do not disclose more diodes connected in parallel to the intrinsic diodes.

Sharples teaches that the parasitic diode is problematic in the case of an insulated-gate field-effect transistor (termed MOSFET). Because this diode is a bipolar component, it is subject

to charge storage effects. It generally has a slow reverse recovery time, which can cause switching losses in operation of the MOSFET. To solve this problem of a slow reverse recovery time, Sharples teaches using a transistor circuit arrangement with an additional external diode of fast recovery time coupled in parallel relationship to the parasitic diode. This fast-recovery diode provides the inverter with a reverse current path external to the MOSFET and in place of the suppressed slow-recovery internal (parasitic) diode of the MOSFET.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to connect an external diode to the source and drains of the MOSFETs in the circuit of Bloomer as taught by Sharples in order to provide a reverse current path external to the MOSFET and in place of the suppressed slow-recovery internal (parasitic) diode of the MOSFET.

12. Claims 15, 16, 18, 20, 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bloomer (US 4,567,425) in view of Bijlenga (US 5,946,178).

Claims 15, 16, 18, 20 and 21; Bloomer discloses an alternating current switching circuit comprising: a first Field Effect Transistor (FET) having a first gate, a first drain, and a common source; a second FET having a second gate, a second drain and the common source; a first diode having a first anode coupled to the common source and a first cathode coupled to the first drain; and a second diode having a second anode coupled to the common source and a second cathode coupled to the second drain. The first gate is coupled to the second gate. The first FET and the second FET are power MOSFETS. The first FET and the second FET are N-type MOSFETs.

However, Bloomer does not disclose a snubber circuit with one resistor in series with one capacitor; wherein the snubber circuit connects the first drain and the second drain.

Bijlenga teaches connecting a snubber circuit across a two transistor-diode circuit; and wherein the snubber circuit comprises one resistor (R2) in series with one capacitor (C2) in order to dissipate excess energy and is also effective with respect to overvoltages.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Suzuki et al in order to utilize one resistor and one capacitor in series and coupled to the first drain and the second drain of the alternating current switching circuit to dissipate energy in the alternating current switching circuit as taught by Bijlenga.

Claim 27; Bloomer discloses a method of switching alternating current comprising: receiving alternating current (AC) from a source; and applying the alternating current across drains of two MOSFET devices of a switch, where the two MOSFET device having a common source region, and their gates are coupled together, and the switch further having diodes that are anti-parallel to each MOSFET device, flowing the alternating current though the common source region.

However, Bloomer does not disclose a snubber circuit connected across the drains. Bijlenga teaches connecting a snubber circuit across a two transistor-diode circuit in order to dissipate excess energy and is also effective with respect to overvoltages.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Bloomer in order to utilize a snubber circuit

connected across the drains of the two MOSFETs in order to dissipate energy in the switches as taught by Bijlenga.

13. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bloomer (US 4,567,425) in view of Sugawara (US 5,635,826).

Claim 22; Bloomer discloses the claimed subject matter in regards to claim 15 supra, except for a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

Sugawara teach using a device (6) having a first pin coupled to the first and the second gate, a second pin coupled to the common source, a third pin coupled to the first drain and a fourth pin coupled to the second drain.

However, the device of Sugawara uses more than four pins since Sugawara is driving two alternating current switching circuits. It is clearly obvious that if Sugawara were to drive only one alternating current switching circuit then only four pins would be required. A first pin would be coupled to the first and the second gate as shown in figure 1, a second pin coupled to the common source as shown in figure 1, a third pin coupled to the first drain (at L1 and coupled through switch 7) and a fourth pin coupled to the second drain as shown in figure 1.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the circuit of Bloomer in order to utilize a four pin device having a first pin coupled to the first and the second gate, a second pin coupled to the common

source, a third pin coupled to the first drain and a fourth pin coupled to the second drain in order to drive the alternating current switching circuit as taught by Sugawara.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,434,019 Baudelot et al disclose that every MOSFET has a parasitic/intrinsic bipolar freewheeling diode reverse-connected in parallel; US 5,682,050 Williams teaches dual MOSFET with parallel diode connection configurations.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on (571) 272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary L. Laxton
Primary Examiner
Art Unit 2838

01/24/2006